LISTING OF THE CLAIMS

1. (Previously Presented) A method for displaying an image by activation of pixels of an array screen based on an image stored in digital form in memory point rows of a frame memory, comprising a normal display mode comprising, for the display of a frame, the steps of:

(a) providing a succession of row addresses associated with rows of the frame memory;

(b) successively reading the states of memory points of the rows associated with the row addresses; and

(c) activating, for each row address, pixels of a line associated with said row address based on the read states of the row associated with said address,

further comprising a stand-by mode comprising replacing step (c) with the steps of:

(d) providing, by a dedicated circuit, at a frequency proportional to the display frequency, a cyclic succession of offset values; and

(e) for each row address of the frame memory, activating pixels of a screen line associated with said address offset by a same pixel position offset value, based on the read states of the row associated with said address, and/or activating pixels of a screen line associated with said row address based on the read states of the frame memory row associated with said address offset by a same pixel position offset value.

2. (Previously Presented) A device for displaying an image on an array screen comprising:

a frame memory comprising memory points arranged in rows and in columns;

a write means for storing in the frame memory an image in digital form;

a read means for reading the states of the memory points of a row of the frame memory at a determined row address;

a row driver for selecting a screen LINE based on the determined row address; and

a column driver for activating pixels of said selected line based on the states of memory points read by said read means,

further comprising:

a dedicated control circuit for providing, at a frequency proportional to the image display frequency, a cyclic succession of offset values; and

a dedicated address circuit receiving the address of the row read by the read means and

transmitting to the row driver a new address corresponding to the address of the read row offset by a same pixel position offset value, and/or a dedicated state circuit receiving the states of the points read by the read means and transmitting to the column driver new states corresponding to the read states offset by a same pixel position offset value.

3. (Original) The device of claim 2, wherein the dedicated state circuit is a shift register, in which are written the states of memory points provided by the read means, adapted to performing an offset by a determined number of bits on said states.

4. (Previously Presented) The device of claim 2, wherein the dedicated address circuit is an adder adapted to adding the pixel position offset value to the address of the read row.

5. (Original) The device of claim 2, wherein the screen is a screen with light-emitting diodes.

6-29. (Canceled)

30. (New) A circuit for shifting a position at which an image is to be displayed, the image being represented by image data comprising a plurality of rows and a plurality of columns corresponding to pixels of the image, the circuit comprising:

a first memory that stores the image data;

a second memory that receives a row of the image data from the first memory and stores the row of image data at first storage locations of the second memory; and

a control circuit that provides a column offset value to the second memory;

wherein the second memory shifts storage locations at which the row of image data is stored based on the column offset value such that the row of image data is stored in second storage locations of the second memory, the second storage locations being shifted with respect to the first storage locations.

31. (New) The circuit of claim 30, wherein the first memory comprises a frame memory that stores image data for an entire image to be displayed.

32. (New) The circuit of claim 30, wherein the second memory comprises a register.

33. (New) The circuit of claim 32, wherein the register comprises a shift register.

34. (New) The circuit of claim 30, wherein the control circuit further provides a column offset direction to the second memory.

35. (New) The circuit of claim 30, further comprising a plurality of column drivers that receive the row of image data from the second memory.

36. (New) The circuit of claim 30, wherein the control circuit provides a cyclic succession of column offset values to the second memory.

37. (New) The circuit of claim 30, wherein the second storage locations are offset from the first storage locations by the column offset value.

38. (New) The circuit of claim 30, further comprising:

a logic unit;

wherein the control circuit provides a row offset value to the logic unit;

wherein the logic unit receives a first row address corresponding to the row of image data and performs an operation on the first row address using the row offset value to determine a second row address that is offset from the first row address.

39. (New) The circuit of claim 38, wherein the control circuit further provides a row offset direction to the logic unit.

40. (New) The circuit of claim 38, wherein the second row address is determined by adding the row offset value to the first row address or subtracting the row offset value from the first row address.

41. (New) The circuit of claim 38, wherein the control circuit provides a cyclic succession of row offset values to the logic unit.

42. (New) A circuit for shifting a position at which an image is to be displayed, the image being represented by image data comprising a plurality of rows and a plurality of columns corresponding to pixels of the image, the circuit comprising:

a first memory that stores the image data;

a logic unit; and

a control circuit that provides a row offset value to the logic unit;

wherein the logic unit receives a first row address corresponding to a row of the image data and performs an operation on the first row address using the row offset value to determine a second row address that is offset from the first row address.

43. (New) The circuit of claim 42, wherein the control circuit further provides a row address offset direction to the logic unit.

44. (New) The circuit of claim 42, wherein the second row address is determined by adding the row offset value to the first row address or subtracting the row offset value from the first row address.

45. (New) The circuit of claim 42, wherein the control circuit provides a cyclic succession of row offset values to the logic unit.